Advanced Research in Electrical and Electronic Engineering
Print ISSN: 2349-5804; Online ISSN: 2349-5812 Volume 2, Number 6 April-June (2015) pp. 62-64

http://www.krishisanskriti.org/areee.html

Automatic Power Factor Correction using FPGA

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Abstract—*This paper presents, automatic power-factor correction using FPGA technology where all the functions can be implemented in a single chip. The implementation tool fit the entered design into the target device (CYCLONE IV). Design verification includes functional simulator, in circuit testing and timing simulation. The main function is to verify the proper operation of the designed circuit. It will compile a design file into a configuration file that is optimized in term of use of logic gates and interconnections for the target device. Power factor measures how effective electrical power is being used. A high power factor means that electrical power is being utilized effectively, while a low power factor indicates poor utilization of electrical power. The simplest way to improve power factor is to add power factor correction capacitors to plant distribution system.*

Keywords: *APFC, FPGA, CLB, ZCD*

1. INTRODUCTION

The power factor of an ac electric power system is defined as the ratio of the real power to the apparent power, and is a number between 0 and 1. Real power is the capacity of the electric load for performing work in a particular time. Apparent power is the product of the current and voltage of the electric load. Low-power-factor loads increase losses in a power distribution system and result in increased energy costs.

In a purely resistive ac circuit, voltage and current waveforms are in phase, changing polarity at the same instant in each cycle. Where reactive loads are present, such as with capacitors or inductors, energy storage in the loads result in a time difference between the current and voltage waveforms. This stored energy returns to the source and is not available to do work at the load. A circuit with a low power factor will have thus higher currents to transfer a given quantity of real power than a circuit with a high power factor [1].

FPGA is a programmable logic device developed by Altera. It comprises of thousand of logic gates. Some of them combined together to form a configurable logic block (CLB). CLB simplifies higher level circuit design, gates interconnections using software are defined through SRAM or ROM. This provides flexibility to modify the designed circuit without altering the hardware part. Concurrent operation, less hardware, easy and fast circuit modification, comparatively low cost for a complex circuitry and rapid protyping make it as the most favourable choice for protyping an ASIC. Automatic power factor correction using different topologies is explained in [1]-[3].

The Automatic Power factor Correction device is a very useful device for improving efficient transmission of active power. If the consumer connect inductive load, then the power factor lags, when the power factor goes below 0.97(lag) then the Electric supply company charge penalty to the consumer. So it is essential to maintain the Power factor with in the limit. Automatic Power factor correction device reads the power factor from line voltage and line current, calculating the compensation requirement switch on different capacitor banks.

2. POWER FACTOR CORRECTION

Power factor correction is the process of compensating for the lagging current by creating a leading current by connecting capacitors to the supply. A sufficient capacitance can be connected so that the power factor is adjusted to be as close to unity as possible [5].

Power factor correction (PFC) is a system of counteracting the undesirable effects of electric loads that create a power factor

that is less than one (1). Power factor correction may be applied either by an electrical power transmission utility to improve the stability and efficiency of the transmission network or, correction may be installed by individual electrical customers to reduce the cost charged to them by their electricity service provider. There are two types of PFCs:
1. Passive 2. Active

There are several advantages in utilizing power factor correction capacitors. These include:

1. Reduced demand charges

2. Increased load carrying capabilities in existing circuits

3. Improved voltage

4. Reduced power system loses

3. AUTOMATIC POWER FACTOR CORRECTION

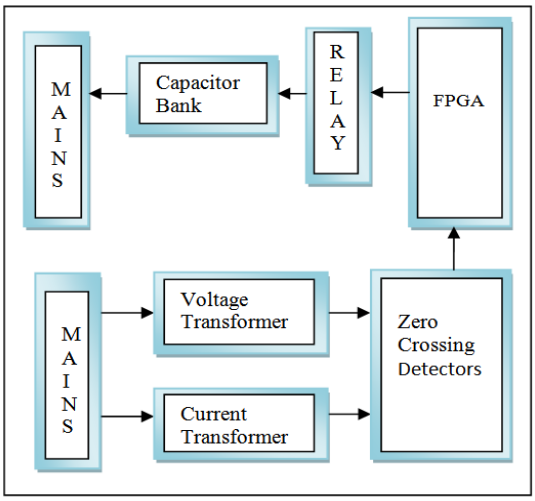

Fig. 1: Block Diagram Configuration

A. Proposed Topology

Basically in this automatic power factor correction module, voltage level should be maintained so that other fault level can be decreased. In controller section FPGA is used so that particular limit for the peak value should be decided and according to that if fault goes above or below that limit the whole circuit will open so that components used in the circuit will be safe and protection of circuit can be easily developed. FPGA is more user friendly than all other controller systems in recent days.

Basically the model of the circuit consist of relay, capacitor bank. The power transformed output from the mains will be fed to ZCD (zero crossing detector) and the output from the ZCD will convert sine-wave to square-wave. The reference voltage in this case is set to zero. The output voltage waveform shows when and in what direction an input signal crosses zero volt. If input voltage is a low frequency signal, then output voltage will be less quick to switch from one saturation point to another. The ZCD output will be driven to FPGA. Where PFC algorithm implemented in FPGA drives the relays and in turn the capacitive bank. The Capacitive bank feeds back PFC output to Mains.

B. Controller development

According to the pin diagram of FPGA controller, it is easy to enter the values of the different section for the varying output and it is also user friendly than the DSP which is being used for the controller. Programming and code generation in the FPGA is according to the fault level and other parameters which are being changed during fault according to the system. FPGA Cyclone IV controller consist of ADC, DAC, Buffer and some other ports are there for the analysis of the power factor correction [4].

4. FPGA CONTROLLER

FPGA controller is a field programmable gate array controller

which works as DSP. Other useful parts are connected with the controller for the proper output.

A. Block diagram analysis

For the analysis of the system, program of FPGA controller provides the feedback for the system which is used to minimize losses as system goes into faulty condition. Program of FPGA controller is the heart of the system for protection or other parameters development. FPGA is more user friendly than the DSP. FPGA controller is also being used as a controller for the protection system development.

Basically the board includes many components system controller which interfaces directly to the configuration LCD control, power monitoring control and other purposes. The system controller contains the required state machine and control logic to determine the configuration source for the controller. For the programming of the controller for one particular system, programming is possible through a serial flash loader and by performing in system programming through the AS programming header [4]. Here FPGA configuration can be done by external USB-Blaster also.

B. Pin configuration analysis

The pin which is being used in the development for the protection system is the CYCLONE IV FPGA. Generally all the components are being operated by this pin. Compressed and uncompressed configuration of data in same program file is possible. Basically compression can be done by enabling bit streams in convert program files. During the system power up, both cyclone FPGA and serial data configuration device enter into a power-on reset mode. The clock pulses which can be generated by the cyclone FPGA controls the entire configuration of the protection system for the power factor correction. Basically this FPGA uses 50MHZ internal oscillator by default to initialize the different values of the parameters. Configuration of multiple devices in a cascading manner is also possible by using a single serial port.

5. SIMULATION RESULTS

So according to the calculation of parameter, voltage and current waveforms can be varied as load changes. Other thing is to be consider as a power factor balancing, PF is maintained throughout the system nearer to unity as much as possible to get desired values so here we are getting PF is around 0.98 which very much nearer to the unity and that shows the ratio of low losses in the system. PF should be in proper manner.

6. CONCLUSION

Here from this concept we can conclude that the power factor correction can be implemented by sensing the voltage and

current waveforms in FPGA Controller and according to that result hardware system is also being implemented.

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